THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

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THIS QPR IS BEING SENT TO YOU BEFORE IT HAS BEEN REVIEWED BY THE STAFF OF THE NEURAL PROSTHESIS PROGRAM.

Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes will have 64 sites of which 8 can be selected for use by the external world. The sites will be buffered on-chip. On one probe the neural signals will then be passed directly off chip, whereas on the other the signals will be amplified, multiplexed, and then passed off chip to minimize external leads. During the past term, we have continued to explore the chronic use of passive recording probes in-vivo. The most recent implant is now 78 days post-op. Neural spike activity is being recorded on one channel. At 51 days, a low-level current was passed from the sites, and this restored activity on two of the channels. The implant will be allowed to continue until no activity can be recorded. It will then be removed and both it and the tissue will be studied to better understand the implant reactions that have taken place on and in the vicinity of the sites.

We have completed the in-vivo testing of probes containing buffers and amplifiers. Probes containing push-pull-type buffers and buffers formed using unity-gain opamps have been used to record activity in-vivo. Like the earlier source-follower probes, these probes had unbuffered (passive) channels located only 24μm (center-to-center) away from the active sites. It is clear that the noise levels of the recordings are not degraded by the presence of the buffers and that the signal quality is as good or better when compared to the unbuffered channels. External noise pickup is of course much better with the buffered channels. The probes containing amplifiers have also been used successfully; however, tests have shown the importance of suppressing the dc offset that can arise at the inputs due to battery voltages arising between the extracellular fluid, the iridium site, and the reference electrode. We clearly see these battery potentials, which can be several hundred millivolts in amplitude and are not being adequately clamped by the small input diodes of the present designs. While such offsets do not trouble the buffers, which have ample dynamic range, they are orders of magnitude larger than neural spike potentials and can saturate high-gain amplifier stages. Suppressing such offsets is particularly important when on-chip data conversion is to be performed, as in probes to be monitored over a telemetry channel. A new input clamping technique using a voltage-variable input resistor has been proposed and simulated for this purpose. We will measure the iridium exchange current density and the input characteristic of our clamping diodes during the coming term to better understand needs in this area.

We also completed the design of the non-multiplexed 64-site 8-channel active probe during the past term. The probe has been implemented in both 8- and 16-shank versions with 200μm site separations. Both 2D (acute) and 3D (chronic) versions are included on the mask set. The probe has a number of modes, including the normal recording mode, site impedance test mode, shank continuity mode, and site activate (dc access) mode. The site selection and mode information can be entered at 2Mhz in 16μsec. We will fabricate this probe during the coming term.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the probe output leads, both in terms of their number and their encapsulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining lead flexibility.

Our solution to this problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of about 300, impedance levels are reduced by four orders of magnitude, and the probe requires only three leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing is in development as is a high-end multiplexed version of this device that includes gain. During the past quarter, work has concentrated in several areas: 1) we have continued efforts to explore chronic recording with platform-mounted "Brain-in-a-Box" passive probes, reaching 78 days with the latest implant; 2) we have concluded acute tests in-vivo using simple active probes containing buffers and amplifiers; 3) we have continued work to integrate a telemetry link with these probes to replace the percutaneous plug now used; and 4) we have completed the design of the non-multiplexed 64-site 8-channel active recording probe. Integration will take place during the coming term. Work in these areas is discussed in the following sections.

2. *Passive Probe Developments*

In the last report, recordings were shown from a chronic "Brain-in-the-Box" assembly (Fig. 1) implanted in guinea pig auditory cortex. It was reported that after an attempt to try to rejuvenate the activity on one of the sites by passing a small amount of current through it, it became evident through high impedances on 8 of the 12 sites that one of the legs of the forked cable broke. The remaining four sites were monitored for one more month and the animal was then sacrificed to retrieve the implant for inspection. As suspected, one of the cable legs did break at the cable junction (Fig. 2). For future implants, this junction will be coated with silastic to enhance mechanical strength.

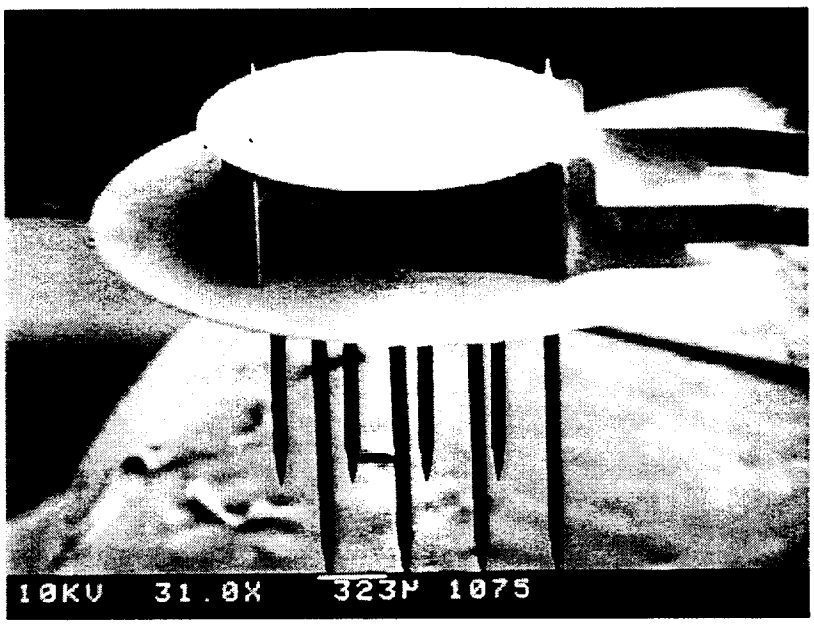


Fig. 1: The 3-D structure known as "Brain in the Box." The two cable strands which are integrated into the probes converge into a single main cable, resulting in the the two probes having sites which face one another. The shanks on this probe are spaced at 300μm.

Another Brain-in-the-Box was implanted in guinea pig auditory cortex during the last quarter. At the time of this writing, the animal has been implanted for 78 days and several of the electrode sites continue to record driven activity. The 1kHz impedance plots for the sites are shown in Fig. 3. The plots are displayed by shank (sites 1-4 are on one shank, sites 5-8 on another, etc.). It appears that there are some common trends, at least on a per-shank basis, with the impedances rather high and varying typically between 4 and 8MΩ. It comes as no surprise that the sites which have recorded activity have done so when their impedances are low. Site 2 developed a short between days 42 and 50 and its impedance remains around 350kΩ.

Throughout the implant period, site 8 has been the best in terms of presence of discriminable units and signal-to-noise ratio. Until day 50, this site had a stable impedance level of about 4MΩ. At this time, activity was not present on any sites. Rejuvenation was attempted on day 51 on sites 1-8 using a 1.5V bias which was current limited through a 20MΩ series resisitor. The impedance levels decreased on sites 5-8, and activity reappeared on several of the sites, including site 1. Since day 51, we have not biased the sites again. The amplitude of the spikes on sites 1 and 8 have decreased. During the

coming days, we will attempt to increase the amplitude of the spikes again through biasing. If this fails, we may sacrifice the animal in an attempt to carefully retrieve the electrode so that detailed optical, and perhaps electrical, analysis of the sites can be performed. Use of the SEM is planned to inspect the sites. We will also perform histological analysis of the tissue. Figure 4 summarizes activity recorded from this chronic preparation.

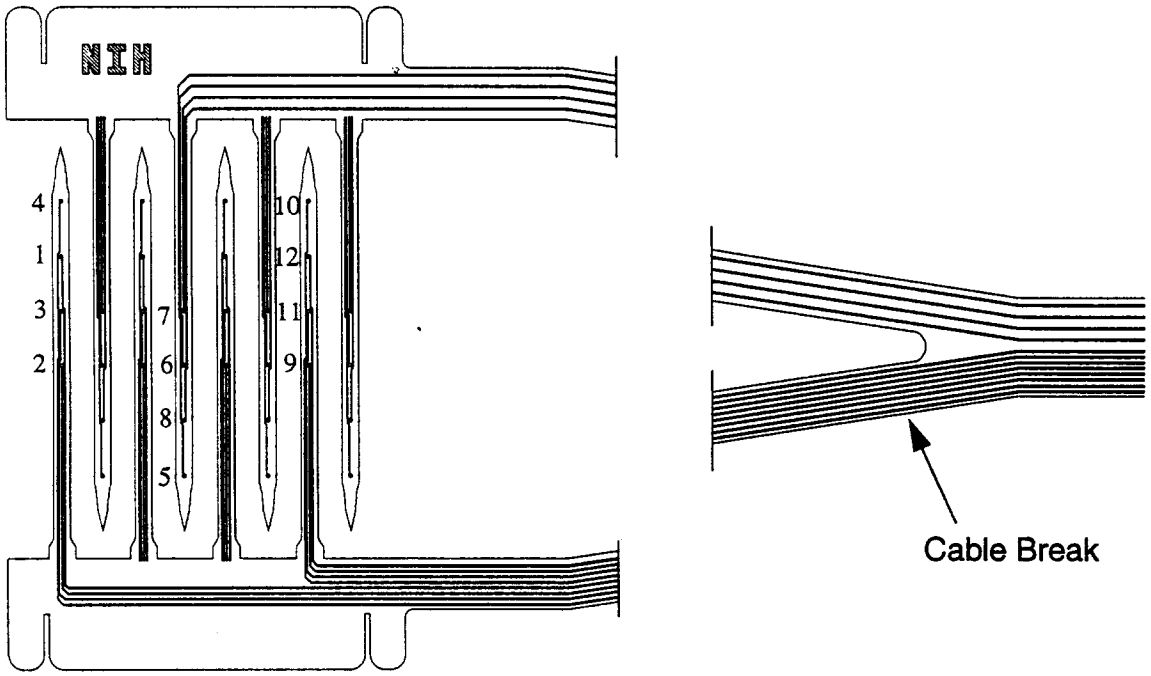


Fig. 2: Schematic of the "Brain-in-the-Box" and location of cable break. This is a particularly vulnerable design to breakage and future implants will have silastic applied at the cable junction to increase the strength there.

3. *Active Three-Dimensional Recording Probe Arrays*

Developing a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses is the goal of this program. It is increasingly clear that for either of these applications, a large number of sites are required in order to make significant progress, which implies that on-probe circuitry is necessary, both to reduce the number of external leads via multiplexing and to reduce crosstalk and noise via buffering and amplification. Thus, a continuing emphasis in this program has been to develop the technology and circuit designs to permit this on-chip circuit integration. As reported in the past quarterly reports, we have made significant recent progress toward this goal, both in the development of a high-yield fabrication process as well as in the design and testing of the resulting 2D and 3D active probes.

Several important accomplishments have been made recently in the area of process development. The process now consistently yields a low contact resistance on all sorts of contacts, including circuit contacts, recording sites and bonding pads. The contact problem had been primarily responsible for the low yields experienced with active probes such as PIA-2. A technique has also been developed to ensure that the active probes are released properly in EDP without having their circuit area being undercut. This technique is based on the use of deep-etched slots around the shanks and wings of the active probes so that

these area are released solely by the front-side silicon etch, leaving thick silicon under the circuit areas. Using dielectric bridges for corner compensation at the outer corners of the circuit areas is also important in protecting the circuit areas from what would otherwise be very rapid EDP undercutting at these corners. Other resolved problems include the improvement of the LTO coverage over the circuit metal; the improved adhesion of gold lead transfers on the 3D arrays; and the use of high-quality dielectric passivation over the interconnects to minimize signal attenuation as well as noise coupling. The full active probe process has now been run successfully with high yield; the active probes realized by the process are being used for testing in-vitro and in-vivo. Active 3D probe arrays have also been created by microassembling finished 2D active probes.

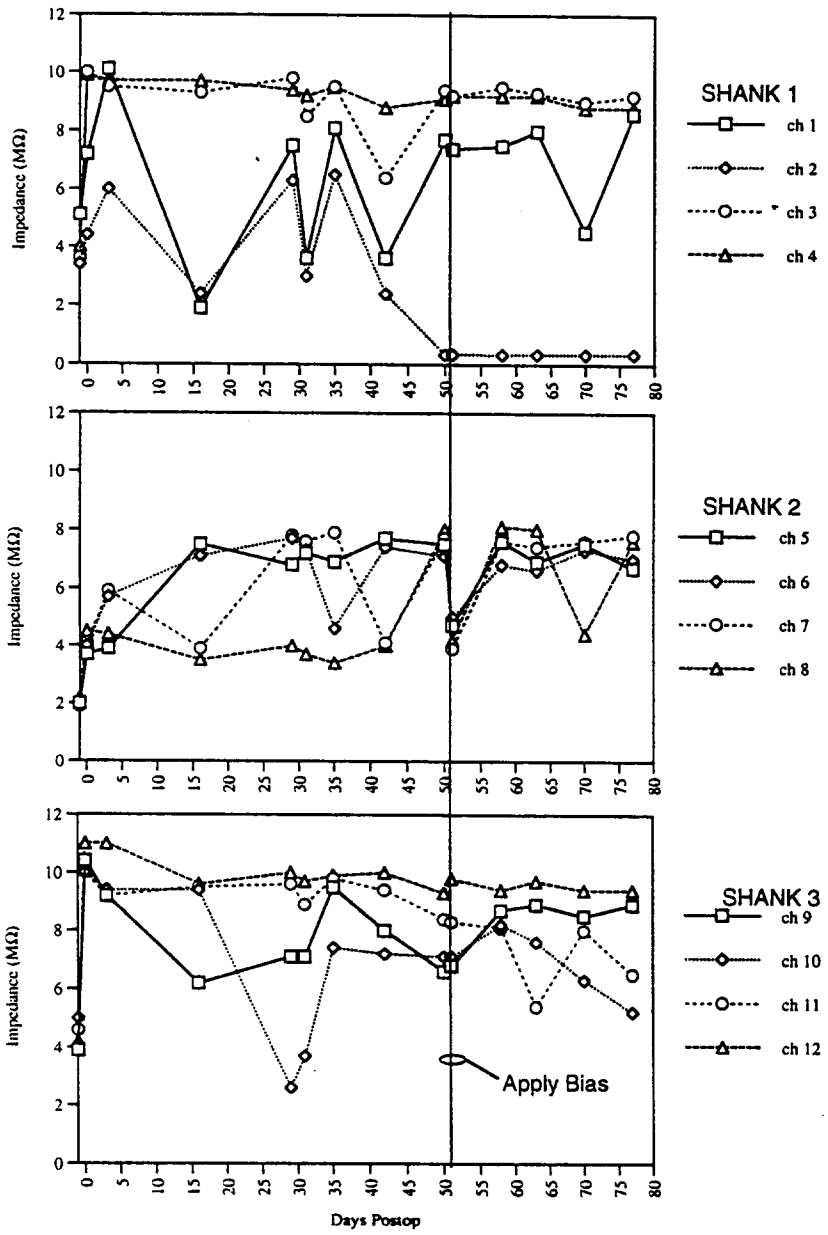


Fig. 3: 1kHz impedance characteristics of a "brain-in-the-box" electrode that is currently implanted in guinea pig auditory cortex. The plots are broken down by the site locations on the three populated shanks.

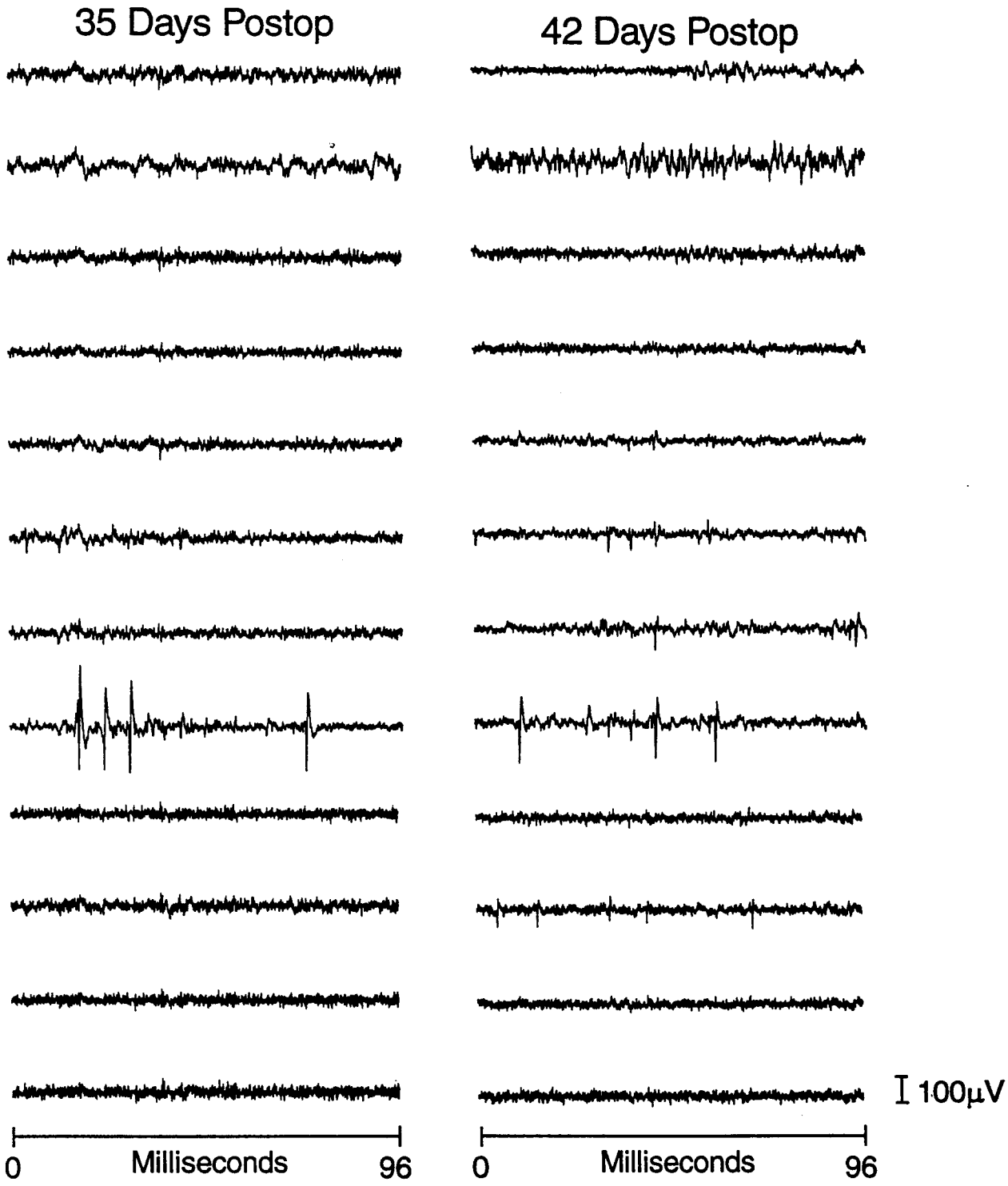


Fig. 4a-b: Activity obtained from brain-in-the-box electrode currently implanted in guinea pig auditory cortex. The responses are driven with a 100msec noise burst. 35 and 42 days post-op.

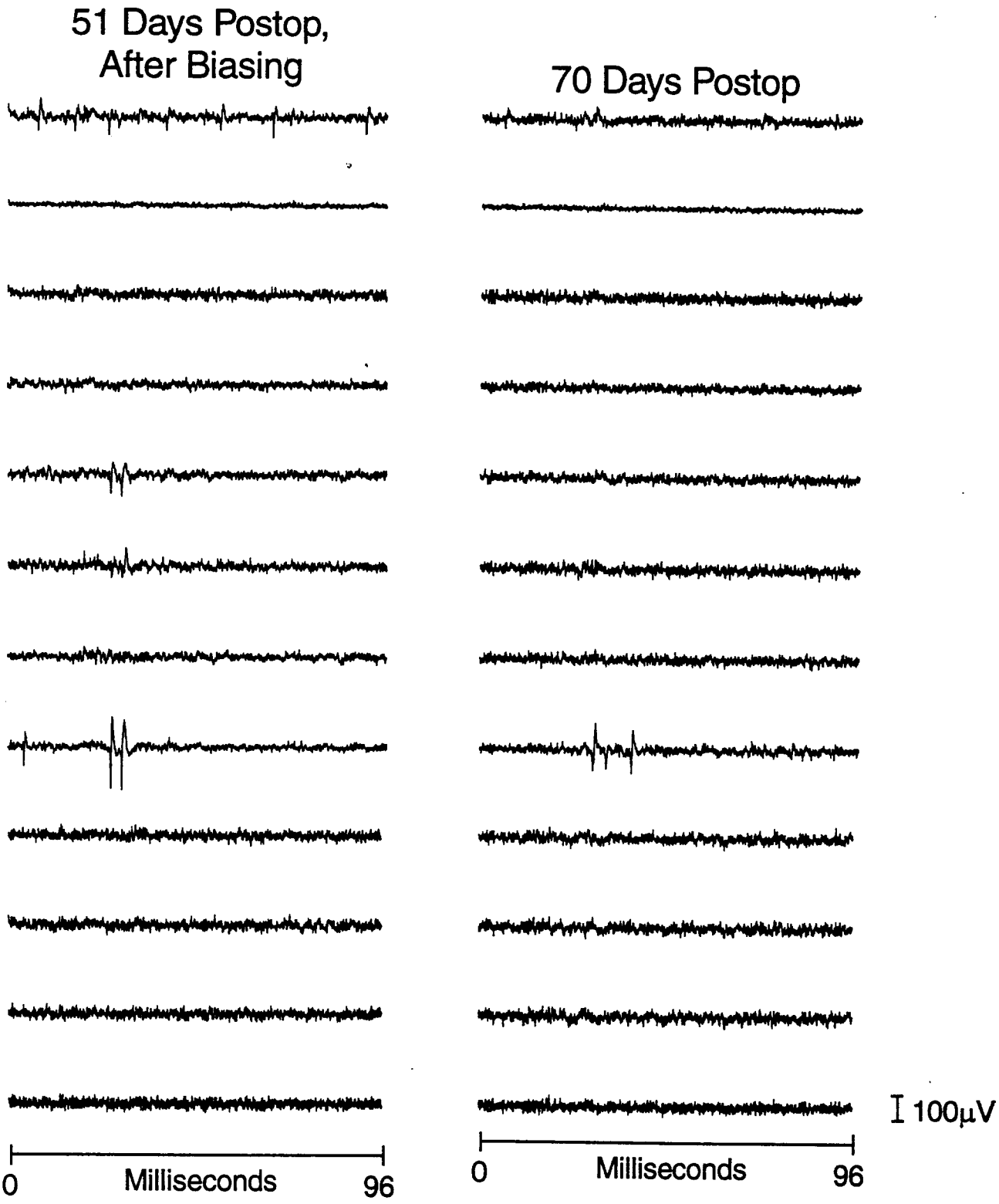


Fig. 4c-d: Activity obtained from brain-in-the-box electrode currently implanted in guinea pig auditory cortex. The responses are driven with a 100msec noise burst. 51 and 70 days post-op.

We have designed and fabricated a set of active recording probes recently in which each probe design tests a certain basic circuit function, including buffering, amplification, and 4:1 multiplexing. The extensive evaluations of these circuit blocks in terms of power, area, noise, and gain, and the detailed study of issues such as dc baseline stability, multiplexer clock noise, and the role of the bias applied to the probe substrate, is setting the stage for the circuit blocks to be used in higher-level probes (PIA 2 and 3) to be integrated later this year. As reported previously, we have now tested some of these active probes. We have also presented successful in-vivo recordings using one of our buffered probes, "BUF1", and one of the multiplexed probes, "MUX1". Probe "BUF1" uses a source follower as the voltage buffer (with a gain of about 0.87), and each buffered channel on the probe has an adjacent unbuffered (passive) channel. The single-unit activity recorded from the active and passive channels on "BUF1" have shown that the noise performance with active channels is not inferior to that of passive channels. Probe "MUX1" has a 4:1 multiplexer and uses an off-chip clock to multiplex the four signal channels that are buffered by source followers. The successful in-vivo recordings with "MUX1" have demonstrated that on-chip multiplexing is feasible with the use of an external clock.

During the past quarter, we have continued testing on other active probe designs. We successfully recorded single-unit responses in guinea pig cochlear nucleus using two of the buffered probes, "BUF2" (a push-pull type buffer) and "BUF3" (a non-inverting unit-gain opamp). We also made recordings with our amplified probes, "AMP2" (open-loop opamp with dc-feedback), "AMP3" (closed-loop opamp with input clamping diode), and "AMP4" (open-loop amplifier with dc-feedback). We have also continued to study the noise problems associated with multiplexed probes.

Recording with Buffered Probes.

In a passive probe, the electrodes are at megohm impedance levels, which puts considerable stress on lead/interconnect encapsulation. Signal attenuation and noise coupling also become more significant when long silicon ribbon cables are used, as in 2D probes and 3D arrays for chronic use. Crosstalk also becomes a concern when stimulation channels and monitoring channels are built together. As a result, on-chip voltage buffers are needed to overcome these problems. It is also feasible to multiplex the buffered recording channels.

We have designed three types of buffered probes. "BUF1" uses a simple source follower. It is robust, typically has a gain around 0.87, and consumes small area but relatively high power. We have successfully applied this probe in in-vivo recordings as reported previously. Another buffer design uses a more complicated non-inverting unity-gain operational amplifier shown in Fig. 5. It has very low output impedance (usually less than 500Ω) and high drive capability, has better noise performance because of its high power supply rejection ratio, and consumes less power (0.25mW in this case). The only drawback of this design is its relatively large layout area, which is 0.075 mm^2. One of the 3D "BUF3" probes is shown in Fig. 6.

As presented in Figs. 7-9, we have successfully recorded single-unit neural spike activity in guinea pig cochlear nucleus using the active probe "BUF3". On this probe, each active (buffered) channel has an adjacent passive (unbuffered) channel below it (the passive one is closer to the probe tip). Both recording sites have an area of 9x9μm^2 and a site impedance of 3 to 4 megohms at 1kHz. The center-to-center site spacing is only 24 μm so that they typically record from the same neurons simultaneously, allowing the noise performance of the two channels to be compared quantitatively. Similar site comparisons have also been made on the probes "BUF1" and "BUF2". Figures 7-9 show that the active

and passive channels have similar levels of noise, although the passive sites seem to have a little more high-frequency noise in Fig. 8. It is clear that the on-chip electronics does not degrade the recordings in terms of noise performance. Indeed, the noise generated by the on-chip electronics is typically less than 15μV-rms over the frequency range of interest (100Hz-10kHz), which is less than the thermal noise from a typical recording site.

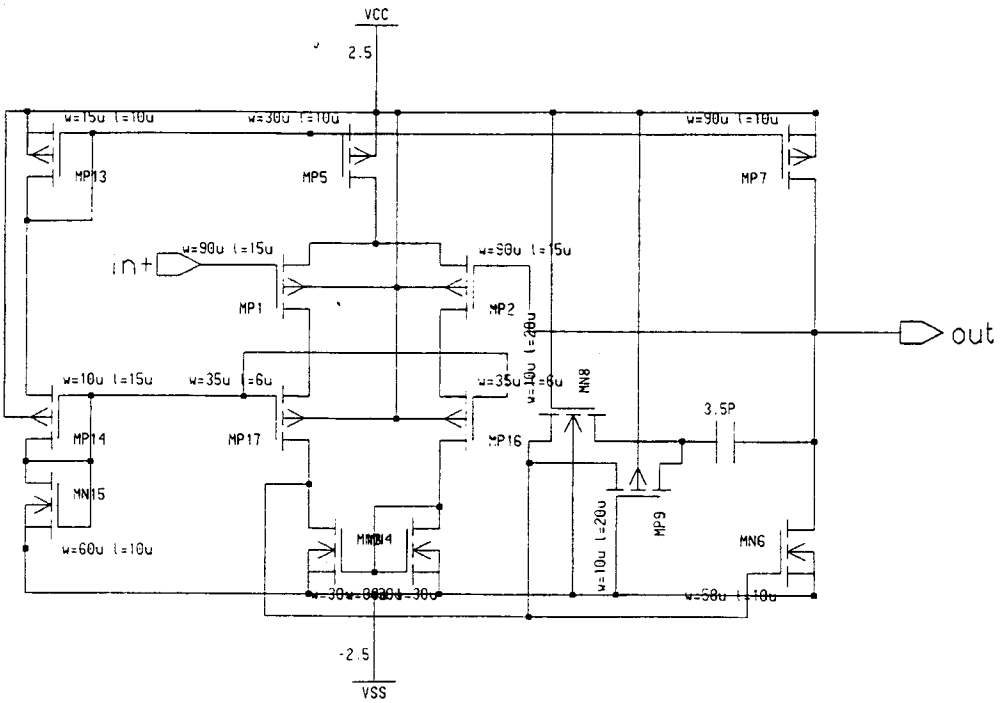


Fig. 5: Schematic of the "BUF3" design, a non-inverting unity-gain opamp.

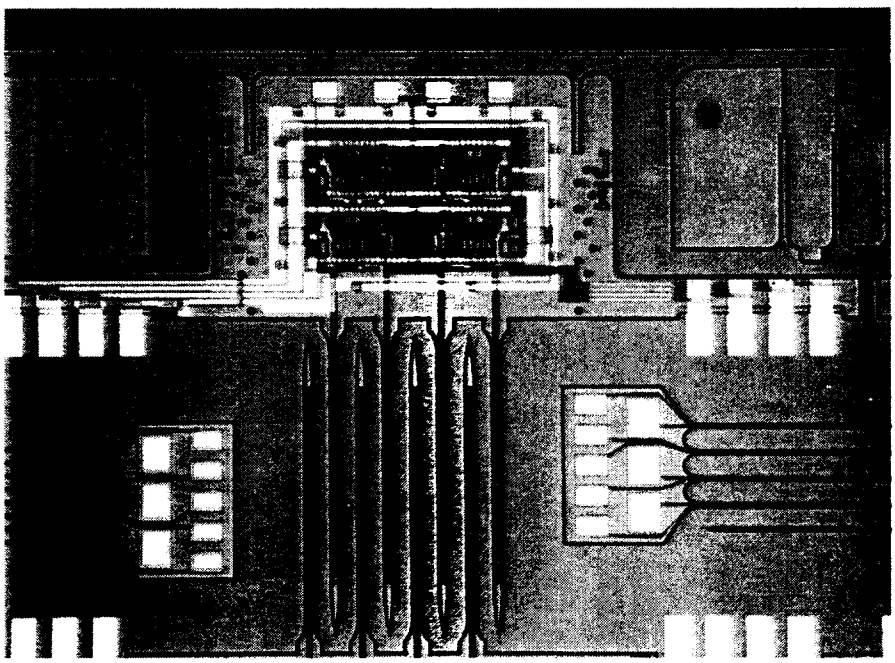


Fig. 6: Picture of the probe "BUF3" before its release from the host wafer.

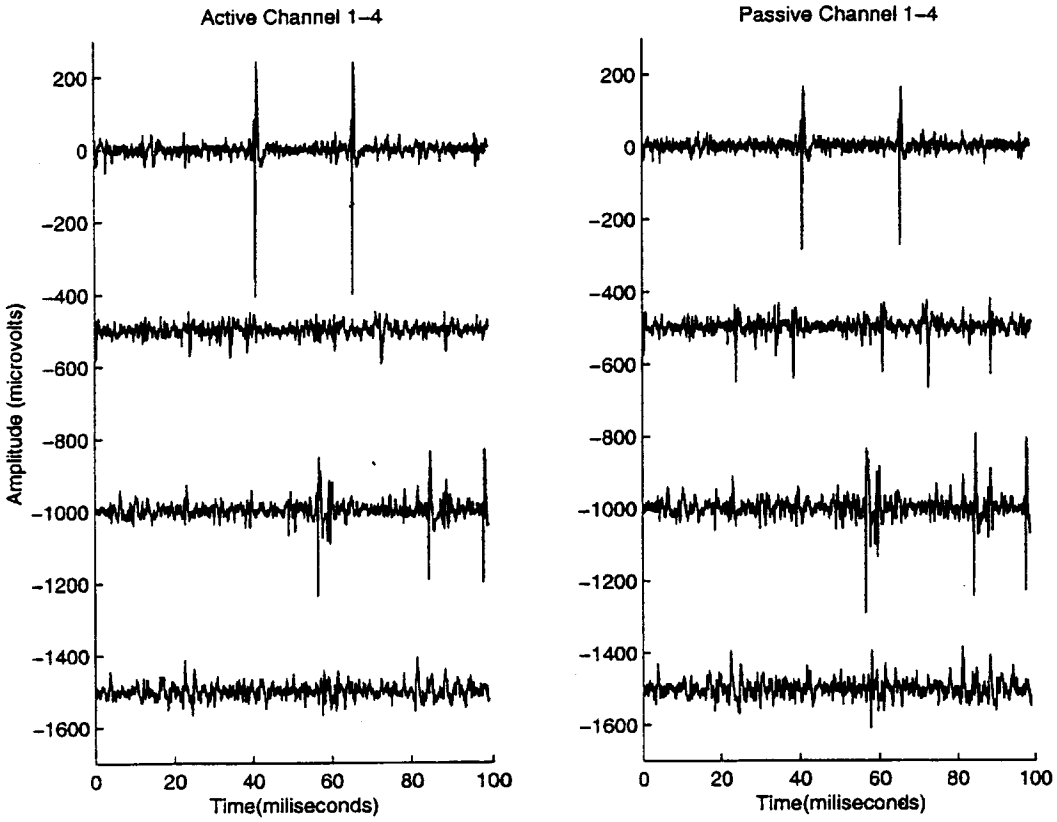


Fig. 7: Single-unit noise-driven activity recorded simultaneously with probe "BUF3" in guinea pig cochlear nucleus. The active channel on each probe shank has a passive counterpart 24 μm below it (center-to-center). And the shank separation is 200 μm.

Even with a 24μm site separation, the active and passive channels may have significantly different spike amplitudes and sometimes even different signal waveforms, depending on the location of the neuron. The previous recording experiments with probe "BUF2" and the experiments with probe "BUF3" have all shown this. As illustrated in Fig. 9, when the probe is moved downward 35μm, cells that formerly were close to the passive site now become closer to the active site, causing increased activity to be seen on that channel. It indicates that the distance over which these cells can be "seen" in cochlear nucleus is no more than about 35μm. It also implies that high-density microelectrodes are needed to fully understand complicated neural networks.

The third design of the buffered probes is "BUF2" is shown in Fig. 10 and is a two-stage push-pull type buffer. Its complexity is in between "BUF1" and "BUF3", and it has an efficiency four times higher than that of "BUF1". But because of its two stages, the gain of "BUF2" is only about 0.7. In-vivo recordings made with probe "BUF2" are presented in Fig. 11. It is noticeable that the active channels have relatively high noise levels compared to those on the probes "BUF1" and "BUF3", probably because the buffer was not biased properly. In fact, in-vitro testing of "BUF2" has shown that its frequency response is noisy and its gain is lower than what it should be. Part of this is due to the fact that the thresholds of the CMOS devices are off the design targets slightly (0.85V for nmos, and -0.65V for pmos). The input dc offset generated at the electrode-electrolyte interface can make this situation even worse.

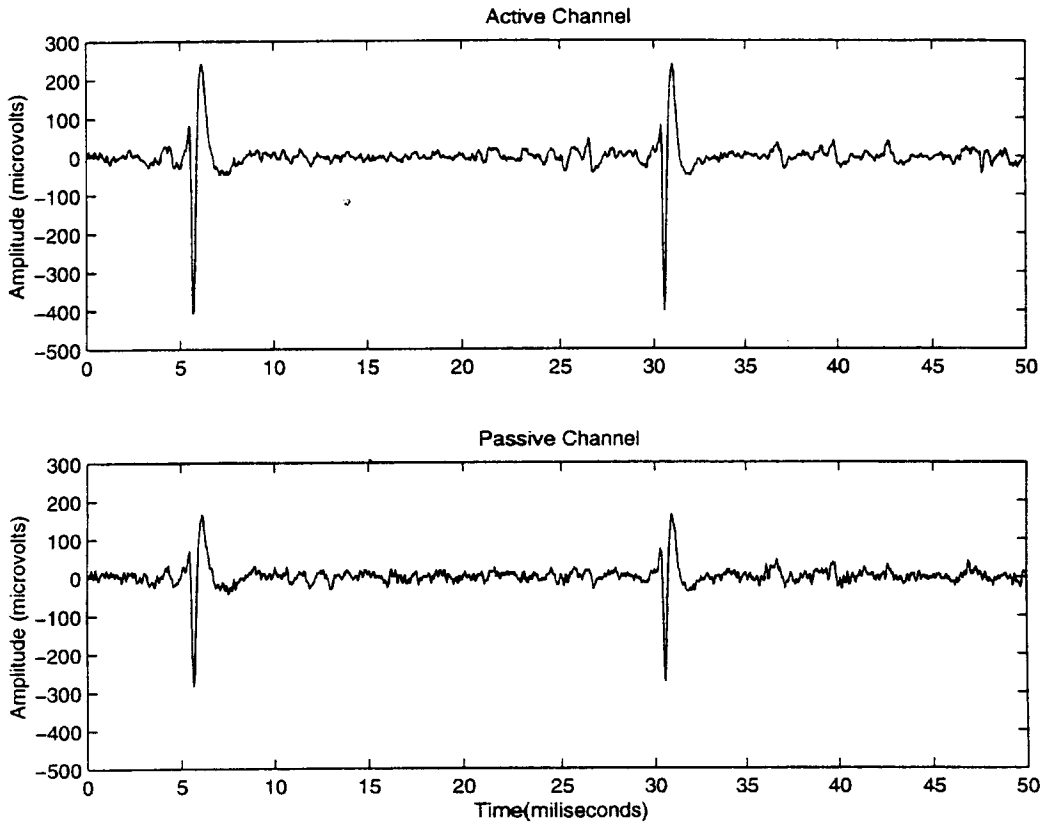


Fig. 8: Close-up view of simultaneous spike recordings from active and passive channels with probe "BUF3".

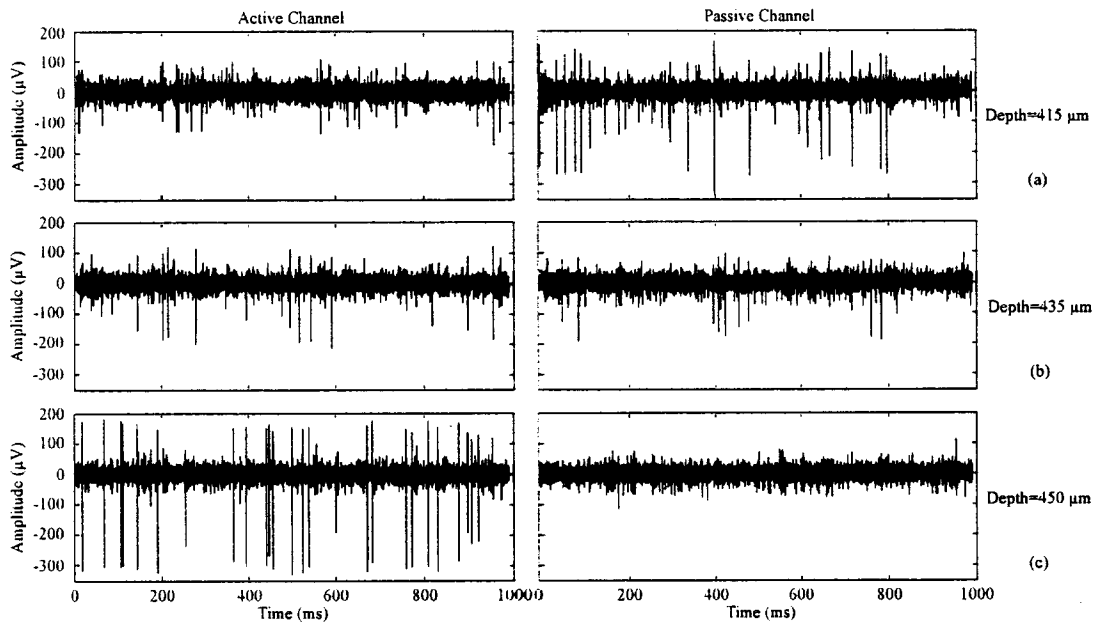


Fig. 9: Single-unit activity driven by white noise burst recorded with probe "BUF3" on the same channels but at different depths.

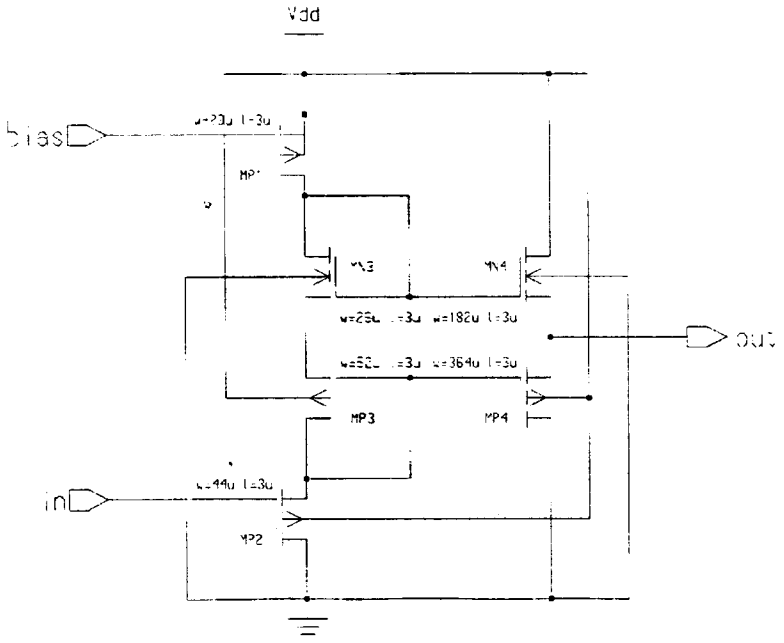


Fig. 10: Schematic of the probe "BUF2" containing a two-stage buffer.

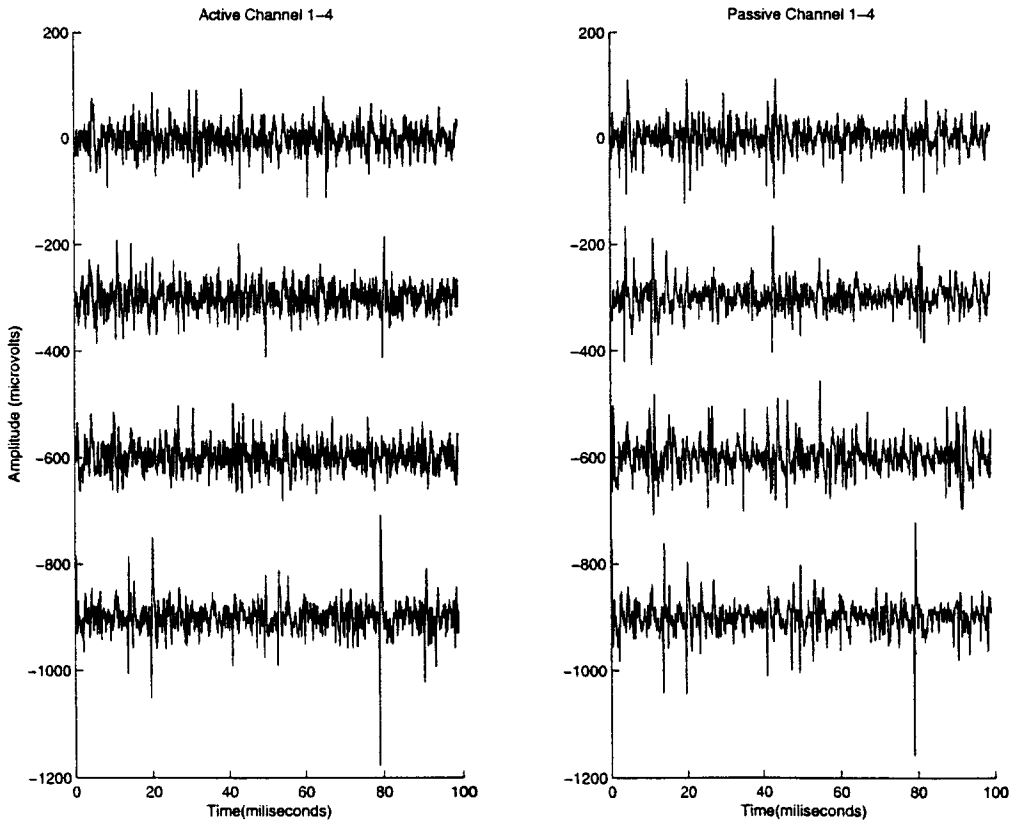


Fig. 11: Single-unit noise-driven responses recorded simultaneously with probe "BUF2" in guinea pig cochlear nucleus.

Recording with Amplified Probes.

There is no doubt that the preamplifiers of active probes should provide stable gains with low noise. However, the dc offsets generated at the electrode-electrolyte interface pose a significant challenge in preamplifier design. Our studies using the probe "BUF3" *in vitro* and *in vivo* have shown that the dc offsets at the circuit inputs using iridium electrodes can be as high as several hundred millivolts. These offsets depend on the site and reference electrode materials used, can fluctuate randomly over time, and can be different in buffered saline than they are in-vivo. Even if the offsets could be balanced, the drift in these levels can easily saturate a high-gain preamplifier, making it important to either reduce the preamplifier gain at dc or clamp the input offset using a passive or active input load device (or both).

Several types of preamplifiers were designed to explore this dc-baseline stability problem. Figure 12 shows the probe "AMP3", a closed-loop amplifier that uses a reverse-biased input clamping diode whose area is $450\mu m^2$. The method of input clamping uses the high junction resistance of the diode near zero bias to polarize the site and eliminate the offset and its associated drift. The challenge here is to provide an input impedance low enough to suppress the dc offsets but still high enough to leave the ac performance of the channel uncompromised. This generally implies a resistance level between $100M\Omega$ and about $10G\Omega$, depending on the exchange current of the site material and the site area.

The diodes used in the amplifier "AMP3" did not adequately suppress the offset since site battery potentials are still clearly seen. The frequency response of "AMP3" presented in Fig. 13 was measured in buffered saline and is very close to the designed/simulated target. But such frequency characteristics could not be obtained all the time due to the fluctuating input dc offset. Depending on the level of saturation, the amplifier gain may decrease dramatically, and the response becomes very noisy. Similarly, gain fluctuations were observed during in-vivo recordings, and the amplified channels became noisier as the gain dropped. In-vivo recordings are shown in Fig. 14 and were made when the gain of probe "AMP3" was very low, indicating a less than optimum bias point.

In order to decide whether the input diode clamp scheme is feasible or not, further studies need to be conducted to characterize the input diode and the exchange current of iridium. The use of a pair of matched diodes connected in parallel but in opposite polarity should be explored, as suggested by the in-vitro and in-vivo experiments: the negative dc offsets were generally less than -150mV; while the positive dc offsets can reach 500mV and beyond. A problem associated with this method is area consumption. Thus, other dc-baseline stabilizing methods should also be explored.

Two of our present amplifiers, "AMP2" and "AMP4", use internal bandlimiting to reduce the gain below 100Hz. Figure 15 is the schematic of the amplifier "AMP2", whose frequency response is illustrated in Fig. 16. As can be seen, the amplifier includes dc-feedback to minimize the effects of dc input offset and drift. The neural responses recorded with the probe "AMP2" are shown in Fig. 17. As reflected by their amplitude scales, the gains of the three amplified channels are somewhat different. This is because the amplifier is open-loop, making the gain susceptible to CMOS threshold variations, and also because of the various dc input offsets. The gain on these recording channels also varied over time during the experiments. In addition, these active channels have relatively high noise levels, which may imply that the dc offsets were so high that they were driving the amplifier into saturation. The neural spike activity shown in Fig. 18 was recorded with the probe "AMP4", a very similar open-loop opamp design with internal dc-feedback.

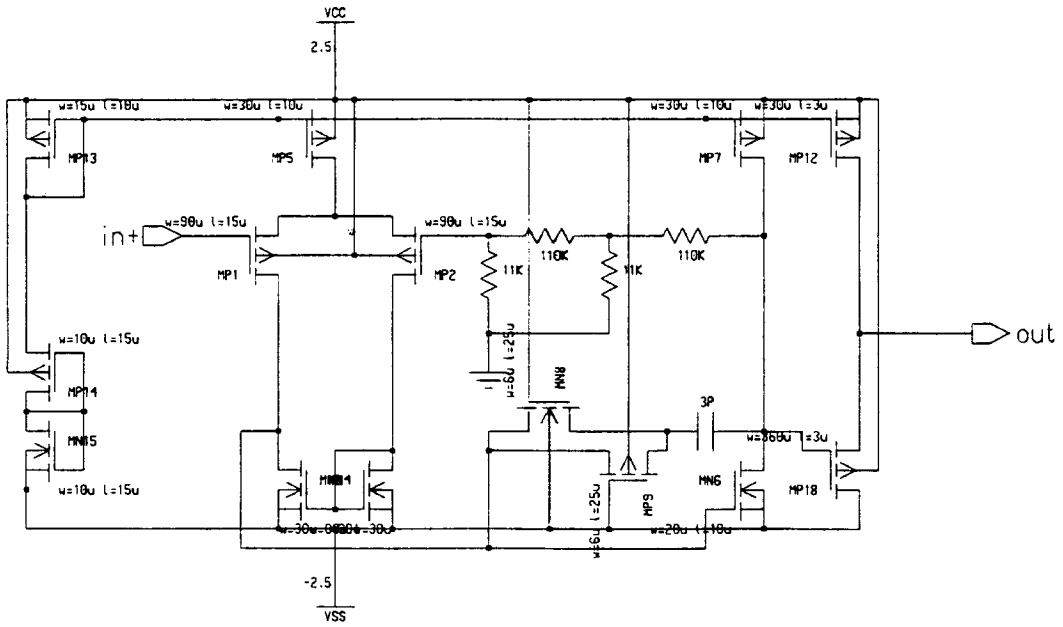


Fig. 12: Schematic of the probe "AMP3", an closed-loop amplifier with an reverse-biased diode at the input.

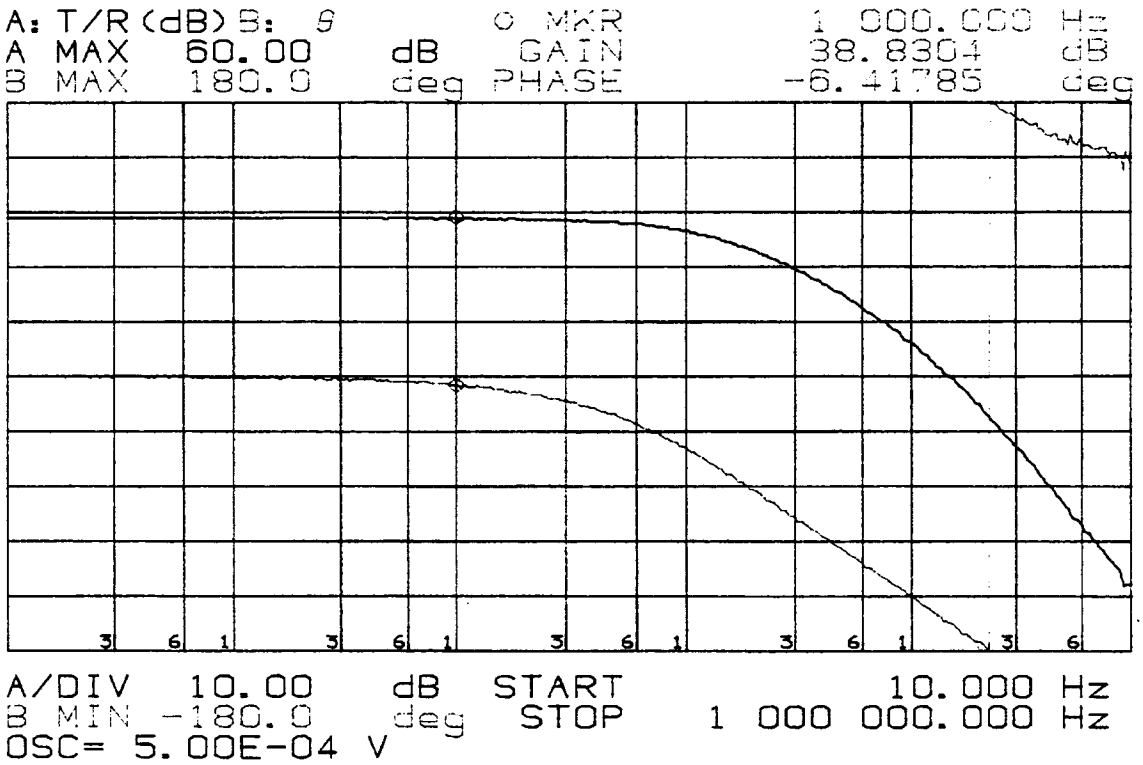


Fig. 13: Frequency response of "AMP3" measured in-vitro.

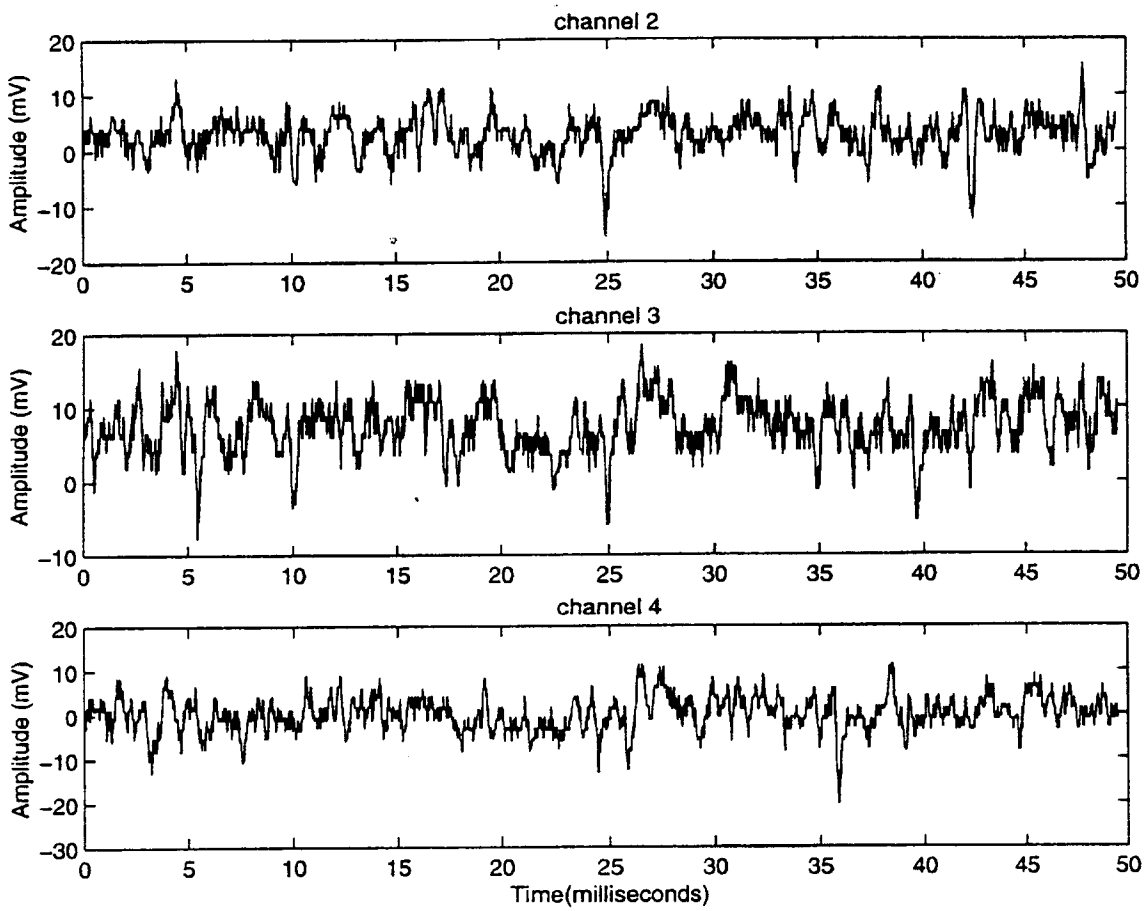


Fig. 14: Simultaneous neural responses recorded with probe "AMP3" in guinea pig cochlear nucleus.

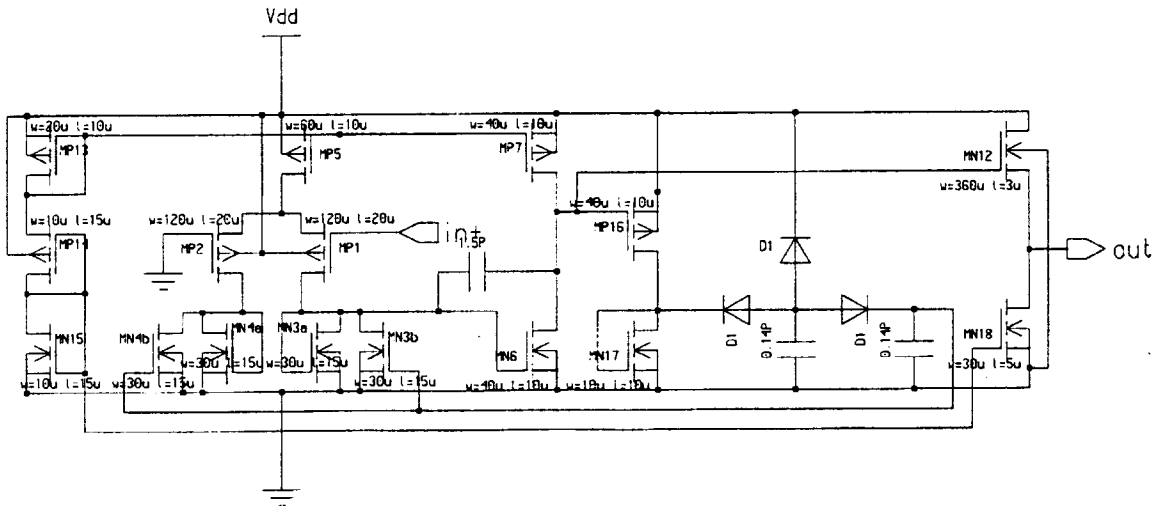


Fig. 15: Schematic of the probe "AMP2" , an open-loop opamp with dc-feedback.

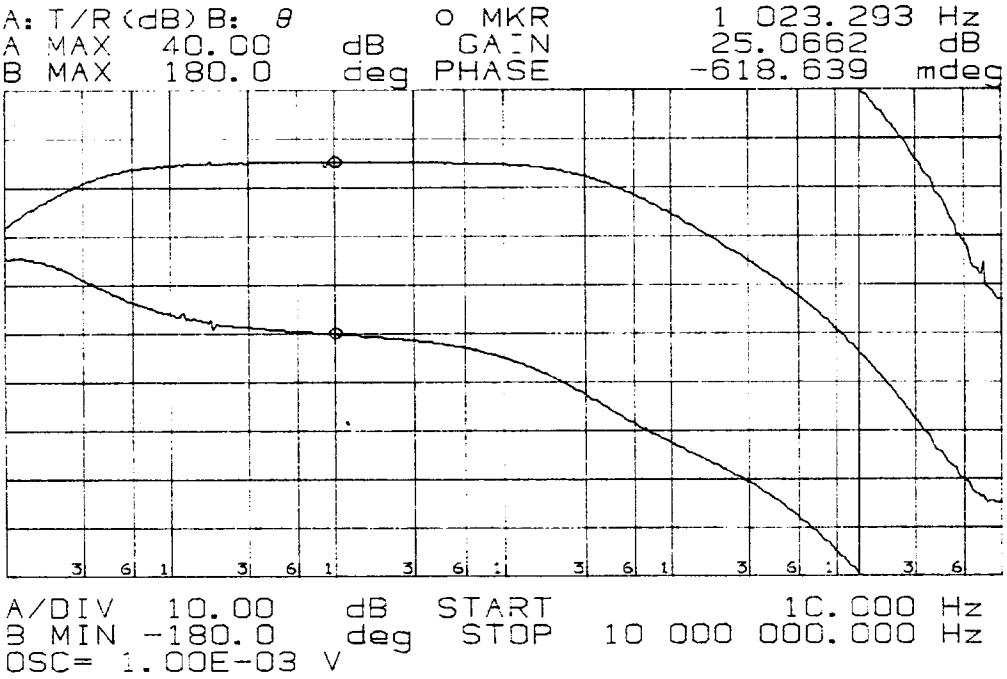


Fig. 16: Frequency response of "AMP2".

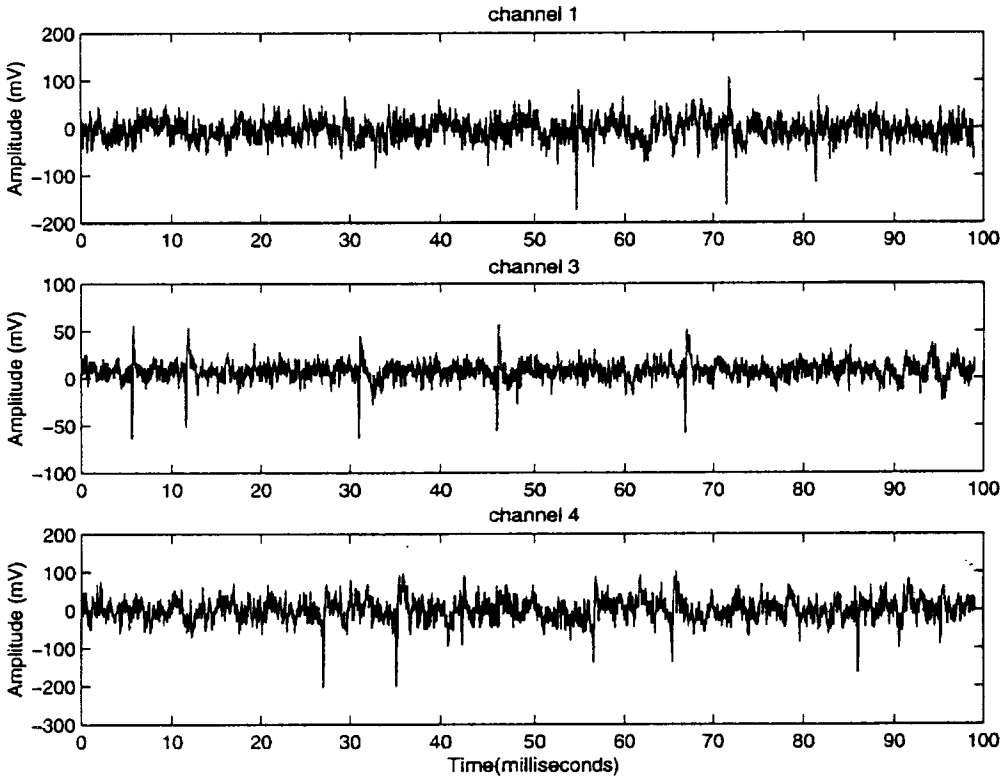


Fig. 17: Single-unit activity recorded with probe "AMP2" in guinea pig cochlear nucleus.

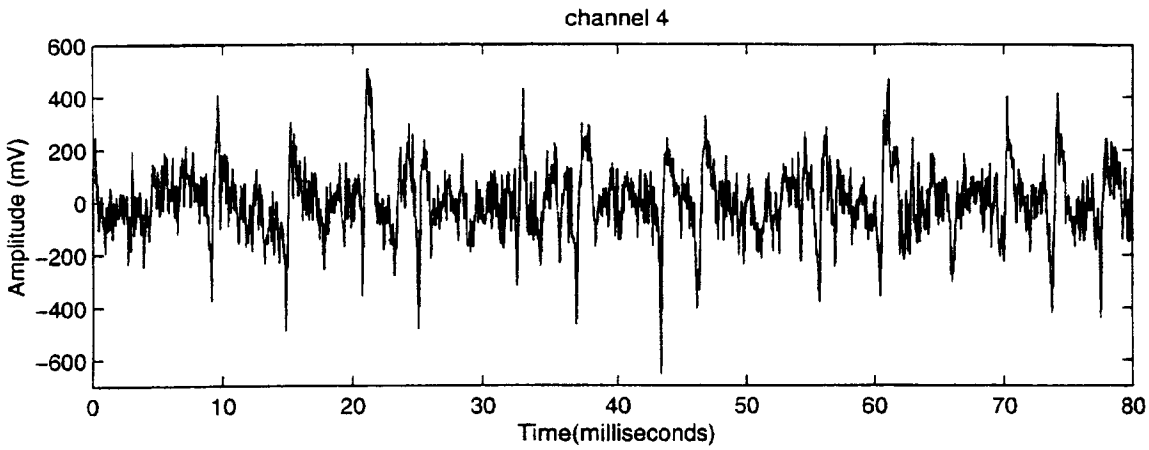


Fig. 18: Single-unit activity recorded with probe "AMP4" in guinea pig cochlear nucleus.

Improving the Noise Performance of Multiplexed Probes.

In the last quarterly report, we reported that significant noise coupling was observed during in-vitro and in-vivo testing with probe "MUX1". One of the noise components is at about 180Hz, while most of the high-frequency noise was at about 10kHz or higher. This noise existed even when the clock to the on-chip multiplexer was shut off. During the recent in-vitro experiments with active probes such as "BUF3", we observed similar noise coupled to the buffered channels when the circuit ground was connected to the earth ground. As a matter of fact, dynamic signal analysis has shown that the noise level can be 6dB higher if the ground reference of the active probe system is connected to the earth ground. The earth ground was used in the experiments with probe "MUX1" because the off-chip clock was generated by a function generator. To avoid noise coupling through earth ground, a clock generator should be built using batteries, completely isolated from the earth ground. Building such a clock generator and other external demux circuits is underway, and we expect to have low-noise neural recordings with the multiplexed probes using these external circuits during the coming quarter.

4. An Integrated Telemetry Interface for Multiplexed Recording Probes

Over the last quarter, work has been started on the development of a 2-channel telemetry module. It is proposed to build at first a simplified version of the system whose architecture was illustrated in the last quarterly report. It is believed that the development of such a system will give us first-hand knowledge of the bottlenecks surrounding circuit design for the module that will stand us in good stead when the final module is developed. The proposed system will demonstrate:

1. Forward Telemetry----the wireless transfer of data and power from an external receiver to the chip. The circuit blocks involved in this are the on-chip receiver coil, the envelope detector, and the clock generator.
2. Reverse Telemetry----the wireless transfer of data from the chip to the external receiver. This process will involve some amount of signal processing on chip in the form of an analog to digital converter (ADC).

It is desirable to develop these circuit blocks in full CMOS technology (unlike the BiCMOS that was previously used for the on chip circuitry in previous designs).

A New Approach For DC Stabilization:

Over the last quarter, we have developed two possible schemes for dc offset suppression at the front end of the recording probe, and these schemes have yielded very encouraging simulated results. One of the most vexing problems in circuit design for neural recording probes has been the fact that the recorded signal has a very large dc component (as much as three orders of magnitude higher than the neural signal itself). This tends to saturate the high-gain preamplifier that is located on the front end of the probe. Also it forces the circuit designs to incorporate a high degree of input voltage range, and this is usually achieved with a decrease in gain /resolution. A number of techniques have been used to try to get rid of the dc offset. These include diode clamps, use of dc feedback, and input reset gates. Some of these were discussed in the previous section. The diode clamps and the DC feedback have to date shown the best results and are in fact used on current active probe designs. However, the current designs are still sensitive to light and leakage currents, and as a result show some instability and nonuniformity.

We are exploring the development of a new active feedback mechanism to eliminate the dc drift in the recorded signal. This ensures that the dc signal is attenuated while the ac signal is amplified. Two designs have been developed, one of which can be used with a dual power supply and the other with a single power supply, as will be discussed below.

Figure 19 shows the schematic of the new DC cancellation scheme using a CMOS pass gate arrangement. The neural signal is represented as an ac signal of amplitude around 10-20μV riding on a dc offset which varies between -150mV and +150mV. Resistance Re and capacitances Ce and Cp model the electrode-electrolyte interface. Typically, Re is in the region of 500 GOhms, while capacitance Ce is about 150pF and capacitance Cp is about 10 pF. The "pass-gate" is used as a voltage-variable resistor in the linear mode.

The ac signal path is set by the high pass RC filter formed between Ce and Cp and the output resistance of the pass gate. On the other hand, the dc signal path is set by the voltage divider formed between Re and the output resistance of the pass gate. Thus, it can be seen that the output resistance of the pass gate is critical in ensuring a good ac and dc performance. The amplifier is represented by A and in this case can operate from a dual supply (e.g., ±5V); hence, the output of the amplifier can be above or below the quiescent value of 0V depending on the polarity of the incoming signal. In case the output of the amplifier is above 0V, then the NMOS device is activated and turns on. When this happens the resistive divider formed between the transistor output resistance and Re attenuates the DC component (because the transistor resistance is much smaller than Re). However, if the output of the amplifier goes negative, then the PMOS device turns on and the DC component gets attenuated. Note that in this circuit, one or the other MOS transistor acts as a resistor whose resistance value is determined by the gate voltage, which is determined by the input DC offset. If there is a large input offset voltage, then the resistance of the MOS transistor will be low since its gate voltage tends to increase. When this happens, the DC offset at the input will be attenuated, as described previously, and thus the circuit will reach an output DC voltage just above the threshold voltage of the MOS transistor. The above circuit was extensively simulated in HSPICE and was found to perform very well. For example, a dc input drift of 200mV was attenuated to 20nV without affecting the ac signal bandwidth or amplitude. The transistors can be of a very small size thus relaxing the area requirement. Furthermore, at any given time only one or the other transistor is on. This dynamic behavior of the circuit is responsible for the low power consumption.

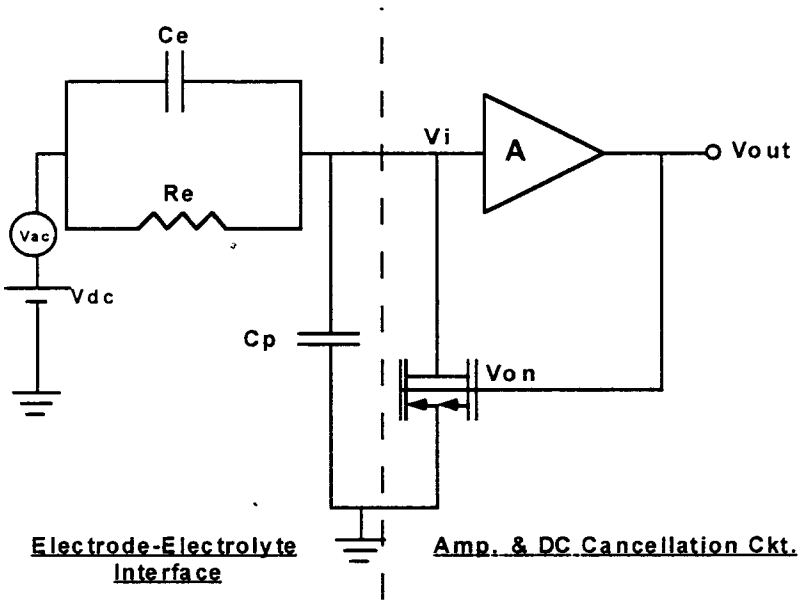


Fig. 19: Diagram showing the basic concept of using active feedback and a MOS transistor to attenuate DC input offset generated by either the electrode or optical currents.

Although this circuit works well and demonstrates that the basic concept of active per-channel feedback is effective, it was decided to modify the above circuit because it needs to operate from a dual supply which is quite inconvenient to generate in a telemetrically operated system. In addition, one needs to ensure that the MOS transistors are always weakly biased so that a lower cutoff frequency of less than 100Hz is always obtained from the circuit. To achieve this, we are now in the process of designing an appropriate feedback scheme that can achieve both of these goals. Although our analysis and design is not completed, we will present preliminary results from one specific circuit approach we are currently pursuing, although there are others we will be studying during the coming quarter.

Figure 20 shows the circuit diagram for the approach that can operate using a single power supply. The operating principle of this circuit is similar to the circuit discussed above. However, this circuit uses a single nMOS transistor and incorporates a feedback circuit in between the gate of the transistor and the output of the amplifier to ensure that this transistor is properly activated. This is achieved by means of a level shifting circuit which ensures that the feedback transistor is always weakly biased.

The operation of the circuit is as follows. Since the output of the amplifier has a quiescent value of around 2.5V and can go above or below this value depending on the nature of the input signal, we have designed a level shifter, shown in Fig. 21, that can operate with an input voltage signal anywhere between 0 V and 5 V and generate an output signal between 0.4 V and 0.85 V. This output voltage is responsible for the weak biasing of the feedback transistor. Due to the weak biasing of the feedback transistor its output resistance is modulated in such a way that it always remains high enough to ensure that the lower cutoff frequency is below 100Hz and low enough to ensure that the dc component of the signal is highly attenuated due to the voltage division with Re.

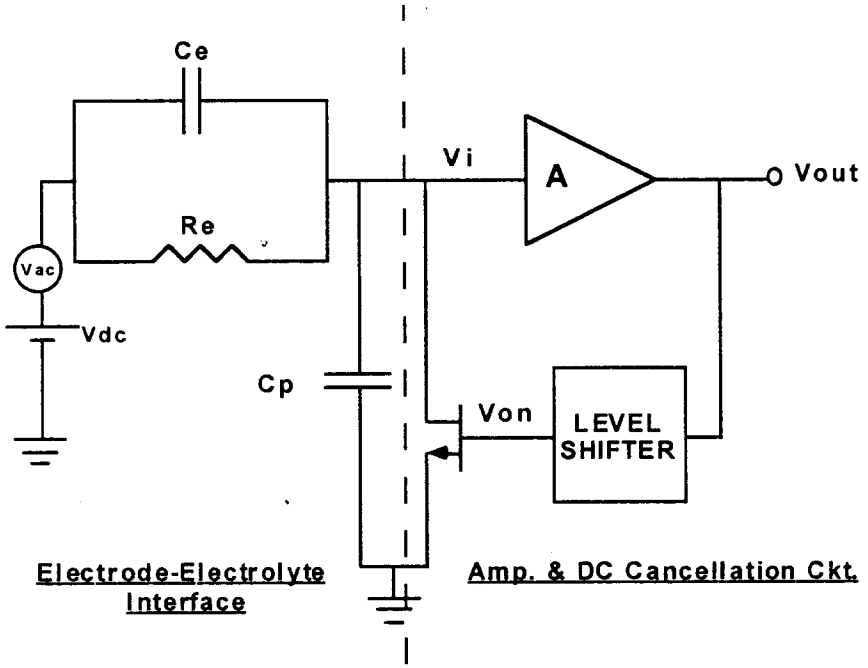


Fig. 20: Circuit diagram for DC offset cancellation using active feedback for operation using a single supply voltage.

This circuit has been extensively simulated during the last three weeks and has been found to work as expected. In simulations a worst case approach was adopted wherein a low ac signal magnitude, and a high dc signal amplitude was chosen. Furthermore, the dc signal was made to drift at a very fast rate (which does not occur in reality) just to test the limits of the circuit. The feedback scheme worked well and the dc component was attenuated to around 50μV (and sometimes to as low as 50nV), while the ac signal was amplified to around 20mV. The amplifier retained a high gain until well over 10kHz. The 3dB frequency for the amplifier used was around 50kHz.

The level shifter employs a diode chain in order to divide down the 5V supply, thus ensuring that the output terminal is always one diode drop above ground. Since the output of the terminal of the level shifter is connected to the gate terminal of the feedback transistor, it can be seen that the feedback transistor is always biased rather weakly. In order to determine the robustness of this arrangement, the process parameters were changed by a large amount and the circuit was simulated in Level 4 HSPICE (in order to account for various processing effects). The circuit operated well up to as much as a 60% change in the process parameters in either direction. Also since the process that is used will affect all transistors of a particular type in the same way, the gate voltage of the feedback transistor will always be at or around the threshold voltage.

Over the next quarter we will continue to perform simulations of both the above circuits and a few other circuit schemes to implement the active feedback approach discussed above. We believe that more optimum and lower-power circuits can be used to achieve this feedback efficiently and these circuits are just now being designed. Once this design and simulation process is completed, a test circuit will be laid out and sent out for fabrication to MOSIS so we can test the robustness and operation of the actual circuit. After this has been completed, work will begin on the circuit design for the 2-channel telemetry system mentioned earlier in this report.

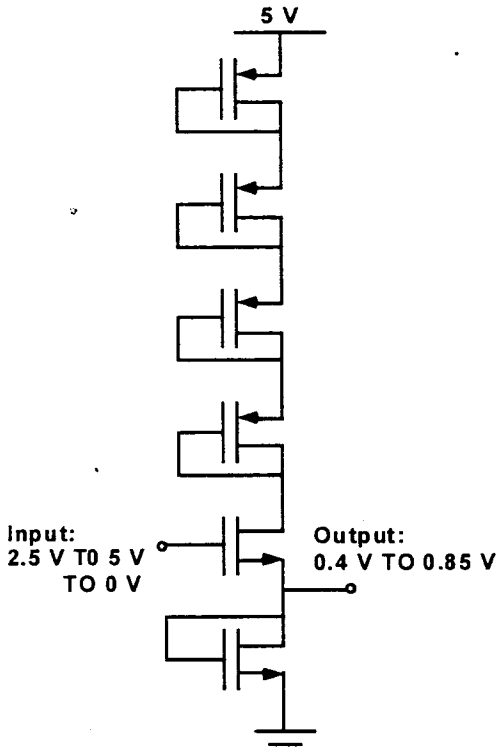


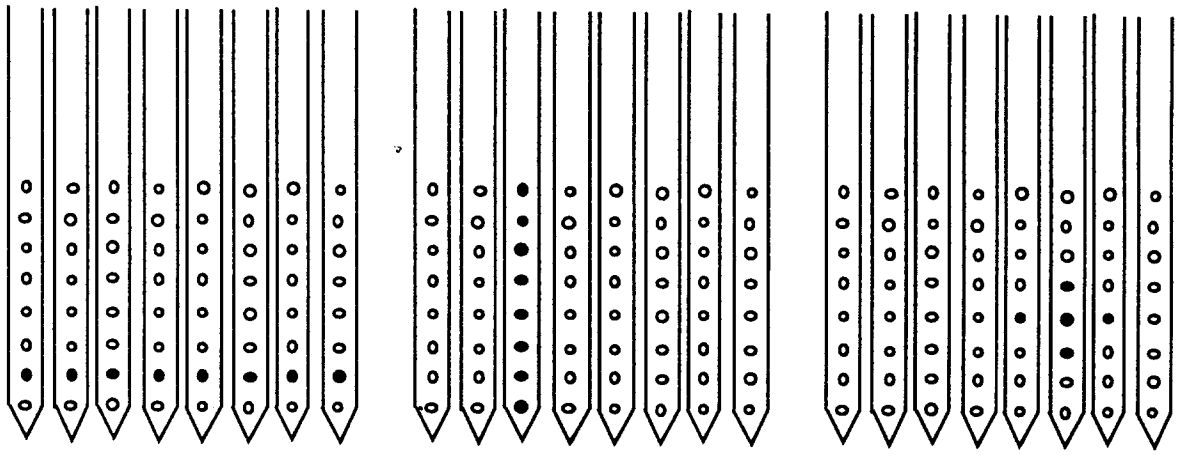
Fig. 22: Circuit diagram of a simple level shifter to generate a low voltage to drive a gate of the feedback transistor.

5. A 64-Site 8-Channel Active Probe

During the past quarter, work was completed on the design, simulation, and layout of a 64 site buffered and front-end selected recording probe. Both 8- and 16-shank versions of the probe were designed, and the 8-shank probe was implemented in both 2D and 3D versions. The probes have 100μm^2 iridium sites, with a 200μm vertical site spacing. The shank spacing is 200μm. The probe has several operational and test modes, which are described below.

In record mode, data from eight of the 64 sites are connected to eight output channels. The sites are wired to the selector circuitry in such a way as to allow depth scans, recording in a vertical slice of tissue, or zooming in a particular area of interest, as shown in Fig. 23. The current site selection is stored in eight three-bit registers, which can be loaded through DATA IN, a serial data channel, in conjunction with an off-chip clock. The probe can also be placed in several test modes. In the shank test mode, the signal from the farthest site on each shank is passed through two separate conductors along the shank to different output channels as shown in Fig. 24. In this way, a DC signal can be passed to ensure continuity along each of the shanks. In the site impedance test mode, a signal can be passed to the sites via the DATA IN channel. A 50fF capacitor acts as a voltage divider with the site impedance, and by measuring the signal on each of the buffered output channels, the site impedance can be deduced. This is illustrated in Fig. 25. The site impedance mode will allow researchers to track site impedance over time and characterize the effects of site conditioning without the need for an impedance analyzer. Finally, in the site activate mode, the buffers are bypassed, allowing DC access to the sites for conditioning. The current operating mode of the probe (record, shank test, site impedance

test, site active) is stored in a three-bit register which is loaded in the same manner as the select registers.



(a) (b) (c)

Fig. 23: Three possible configurations of selected sites. a) Depth scan b) vertical slice c) area zoom.

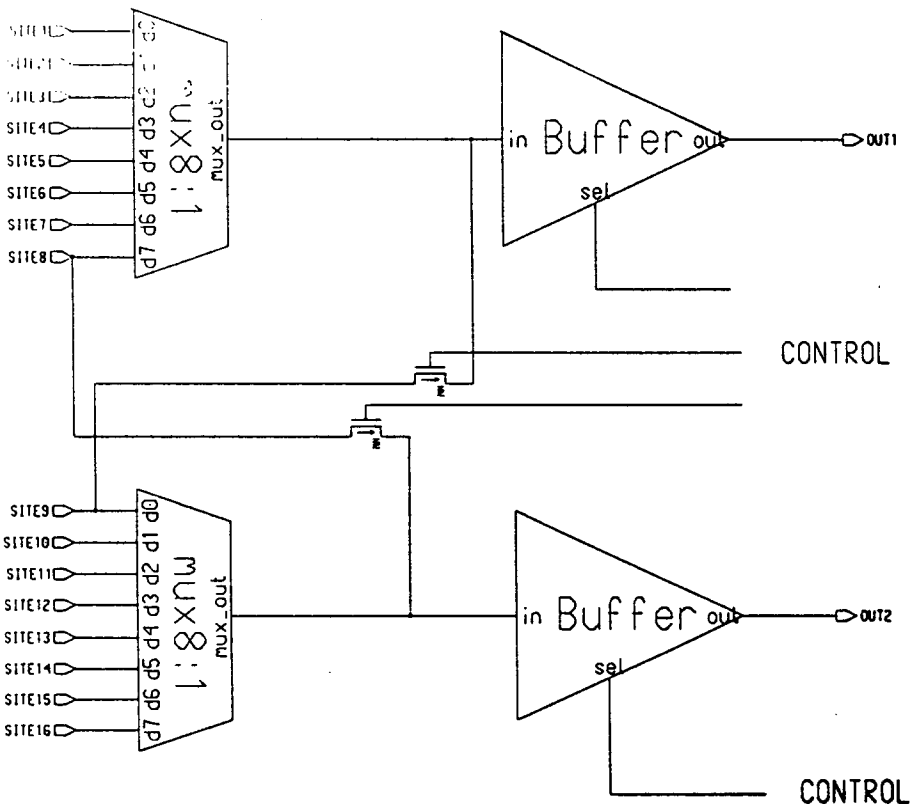


Fig. 24: Shank continuity test; the site nearest the shank tip is connected to separate outputs via different conducting paths. The buffers are switched out and the NMOS transistors are switched on by the control lines shown.

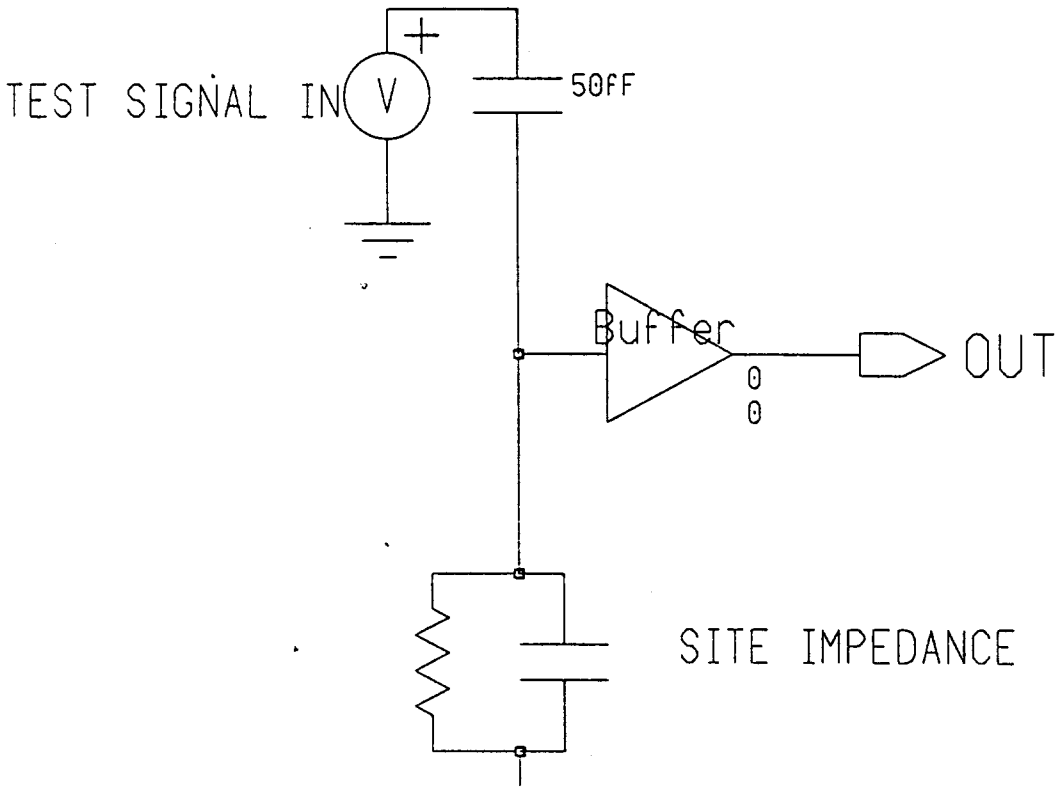


Fig. 25: Site impedance test; measurement of site impedance with test signal input.

Simulations were carried out on both the analog and digital portions of the probe. The shift registers were implemented with edge-triggered D flip-flops which have been described elsewhere (see Quarterly Report #3, p. 12) and are latched into simple SRAM cells with the receipt of the final data bit, at which time a "data received" pulse is output on the DATA IN line. This design permits recording to continue during the programming of the probe, allowing the possibility that the front-end selector could actually be used in a multiplexer mode. Simulations which include the parasitic capacitances extracted from the layout show that the registers can be loaded with a clock rate of at least 2MHz, corresponding to a total time for programming of 16μsec. Simulations show that the cross channel coupling through the NMOS select switches is negligible. While the coupling of the clock to the data channels during programming is visible, it is limited to the edges of the sampling windows. In addition, the clock will not normally be active during record mode. The buffer used in this probe is the (unity gain) source follower implemented successfully on the probe BUF1; it has an output impedance of 10-20kΩ.

The layout of this probe is given in Fig. 26. The layout integrates our most up-to-date process technology based on knowlege gained from other probe designs. This includes corner compensation and vertical slots for release in EDP without damaging active circuitry, a 2 poly process for capacitor implementation, and the revised process for contact to circuit areas and sites.

This probe is a first step towards addressing the need for active probes with large numbers of recording sites. It will be a good starting point for the next generation of probes, which will be front-end selected, amplified, and multiplexed. The buffers found on this probe will be replaced with an amplifier circuit block, and the eight output channels will be multiplexed onto a single output channel, which can be implemented by adding a multiplexer and clock input to the rear of the existing probe. The knowledge we have

gained through the design of multiplexed active probes as described in section 3 will be used in the design of the multiplexer in order to minimize clock feedthrough and other noise sources. Processing of this probe is expected to be completed in the coming quarter.

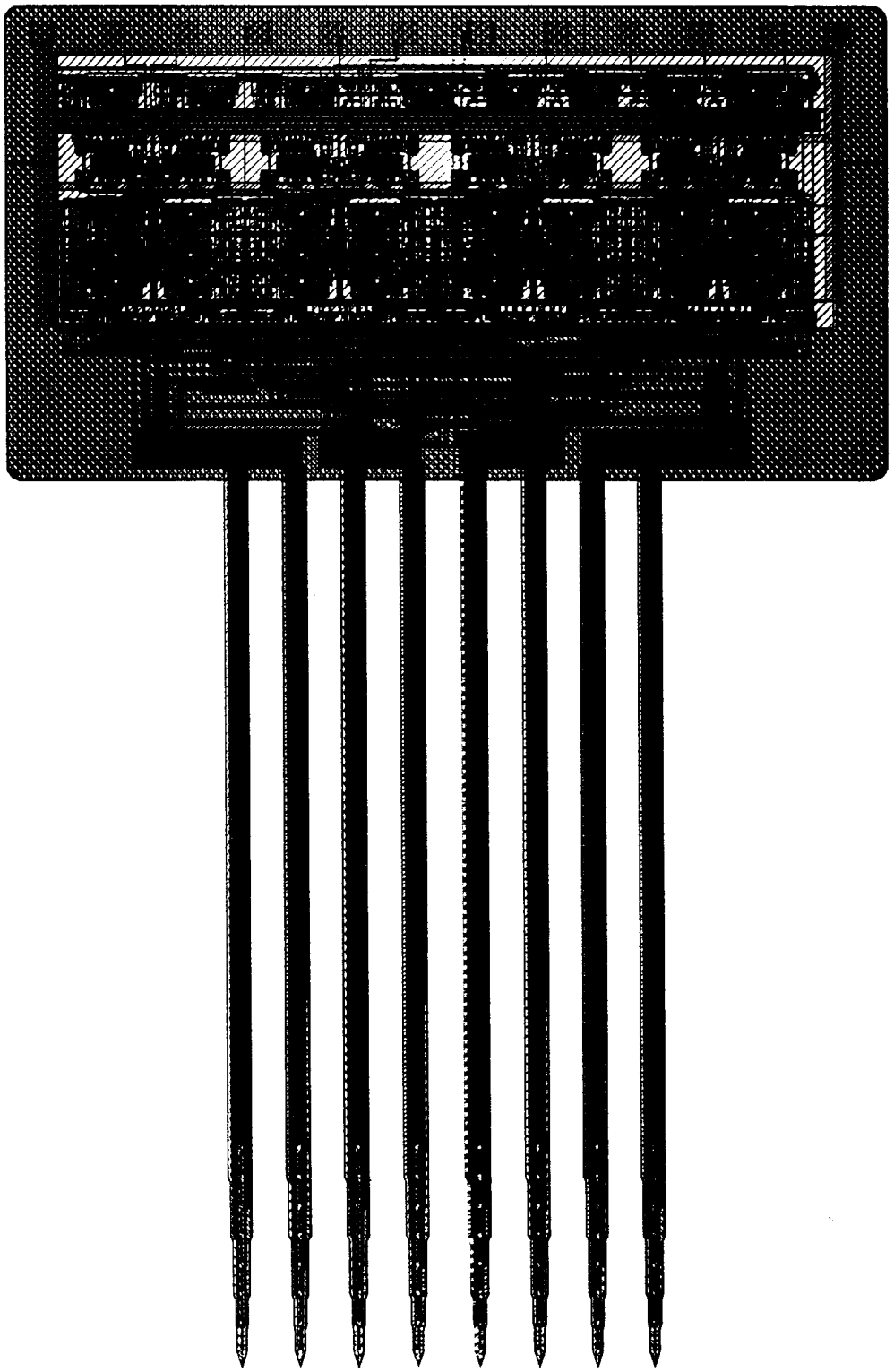


Fig. 26: Layout of the 8-shank non-multiplexed 64-site acute probe.

6. *Conclusions*

The goal of this contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes will have 64 sites of which 8 can be selected for use by the external world. The sites will be buffered on-chip. On one probe the neural signals will then be passed directly off chip, whereas on the other the signals will be amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) configurations of these probes are being developed.

During the past term, we have continued to explore the chronic use of passive recording probes in-vivo. The most recent implant is now 78 days post-op. Neural spike activity is being recorded on one channel. At 51 days, a low-level current was passed from the sites and this restored activity on two of the channels. The implant will be allowed to continue until no activity can be recorded. The implant will then be removed and both it and the tissue will be studied to better understand the implant reactions that have taken place on and in the vicinity of the sites.

We have completed testing of probes containing buffers and amplifiers. Probes containing push-pull-type buffers and buffers formed using unity-gain opamps have been used to record activity in-vivo. Like the earlier source-follower probes, these probes had unbuffered (passive) channels located only 24μm (center-to-center) away from the active sites. It is clear that the noise levels of the recordings are not degraded by the presence of the buffers and that the signal quality is as good or better when compared to the unbuffered channels. External noise pickup is of course much better with the buffered channels. The probes containing amplifiers have also been used successfully; however, tests have shown the importance of suppressing the dc offset that can arise at the inputs due to battery voltages arising between the extracellular fluid, the iridium site, and the reference electrode. We clearly see these battery potentials, which can be several hundred millivolts in amplitude and are not being adequately clamped by the small input diodes of the present designs. While such offsets do not trouble the buffers, which have ample dynamic range, they are orders of magnitude larger than neural spike potentials and can saturate high-gain amplifier stages. Suppressing such offsets is particularly important when on-chip data conversion is performed, as in probes to be monitored over a telemetry channel. A new input clamping technique using a voltage-variable input resistor has been proposed and simulated for this purpose. We will measure the iridium exchange current density and the input clamping characteristic of our clamping diodes during the coming term to better understand needs in this area.

We also completed the design of the non-multiplexed 64-site 8-channel active probe during the past term. The probe has been implemented in both 8- and 16-shank versions with 200μm site separations. Both 2D (acute) and 3D (chronic) versions are included on the mask set. The probe has a number of modes, including the normal recording mode, site impedance test mode, shank continuity mode, and site activate (dc access) mode. The site selection and mode information can be entered at 2Mhz in 16μsec. We will fabricate this probe during the coming term.